1/13

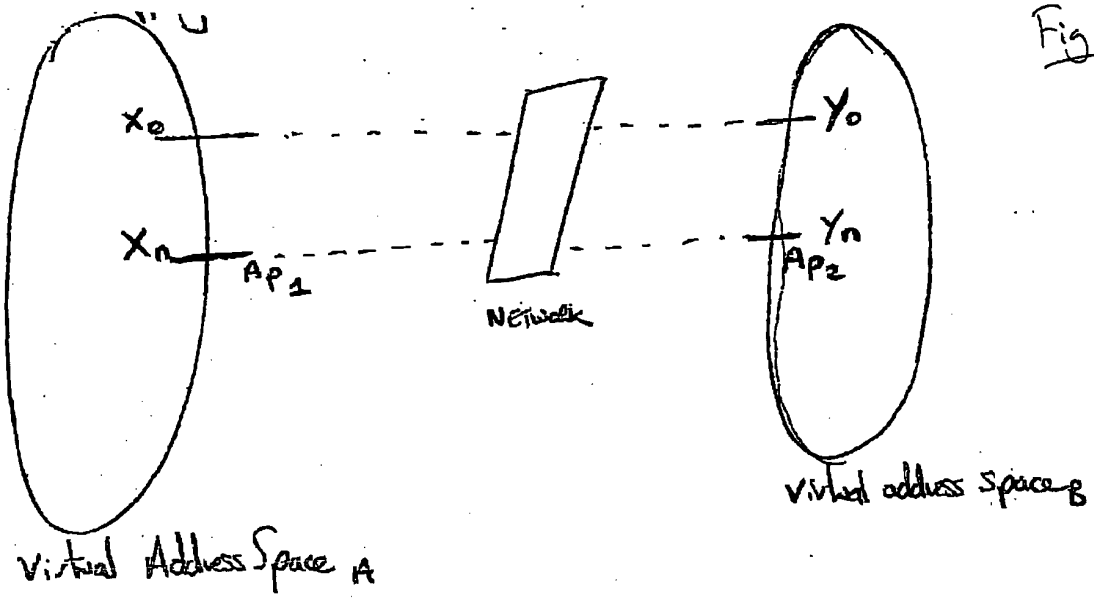
X_0
X_n
AP_1
Network
Y_0
Y_n
AP_2
Virtual Address Space A
Virtual address Space B

Fig. 1

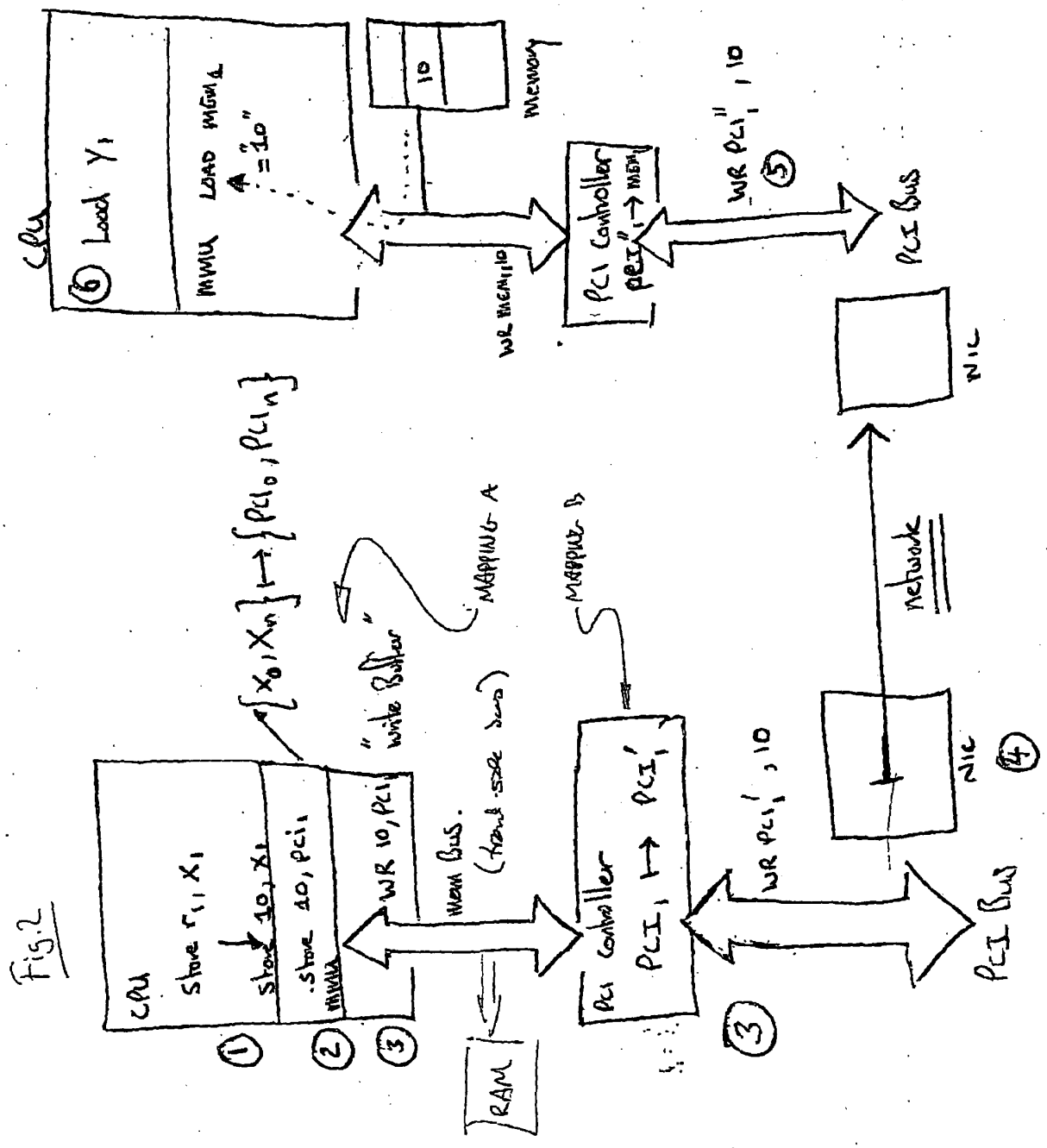
CPU
Store r1, X1
store 10, X1
store 40, pci1
MMIA
WR 10, pci1
"write Buffer"
Mem Bus.
(Host-side bus)
RAM
PCI controller
PCI1 → PCI1'
WR pci1', 10
PCI Bus
NIC
network
NIC
MAPPING A
MAPPING B
{X0, Xn} → {pci0, pci n}
CPU
Load Y1
MMIA LOAD MMIA
A = "10"
10
Memory
WR MEM1,10
PCI Controller
pci1 → MEM
WR pci1'', 10
PCI Bus
1
2
3
3
4
5
6

Fig. 2

Fig 3

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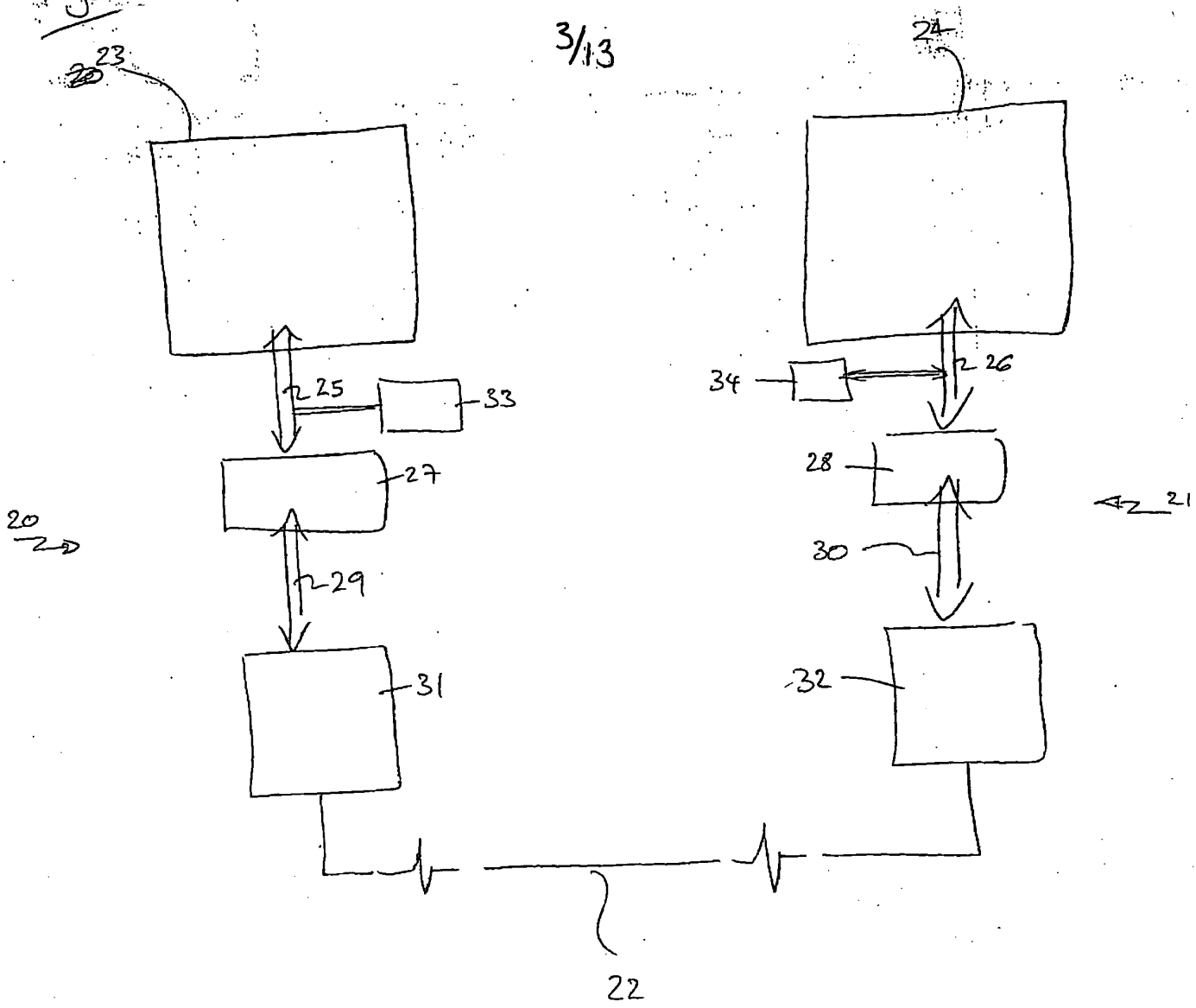

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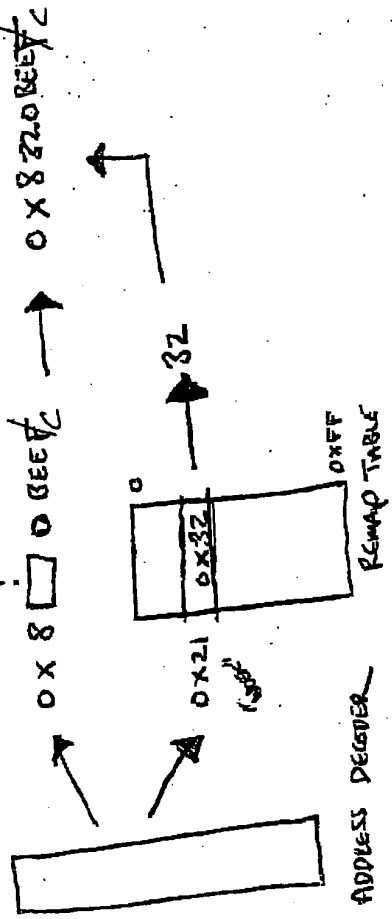
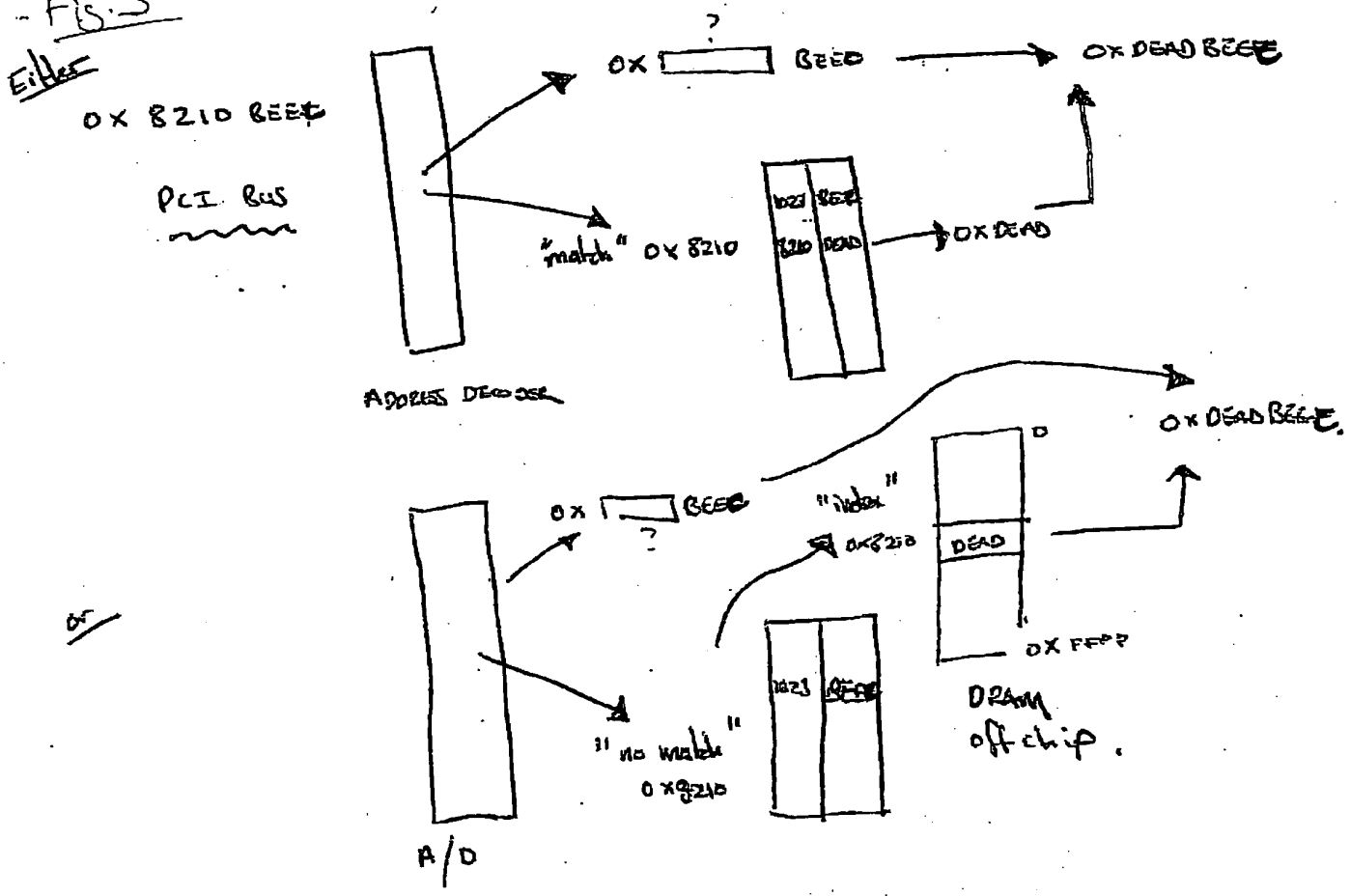


Fig 4
0X8210BEEFC

Fig. 5


Either
0x 8210 BEEF
PCI Bus
0x ? BEEF
0x DEAD BEEF
"match" 0x 8210
0x DEAD
Address Decoder
0x DEAD BEEF
0x ? BEEF
"index"
DEAD
0x FFFF
DRAM
off chip.
"no match"
A/D

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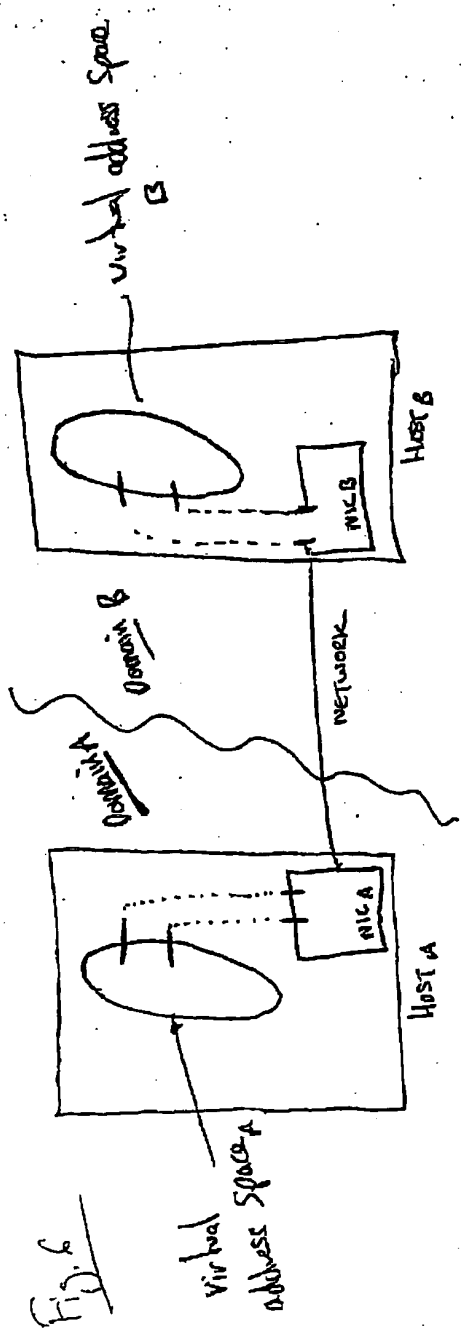
Virtual address Space B
HOST B
NIC B
Domain B
Domain A
NETWORK
NIC A
HOST A
Virtual address Space A

Fig. 6

Fig.7

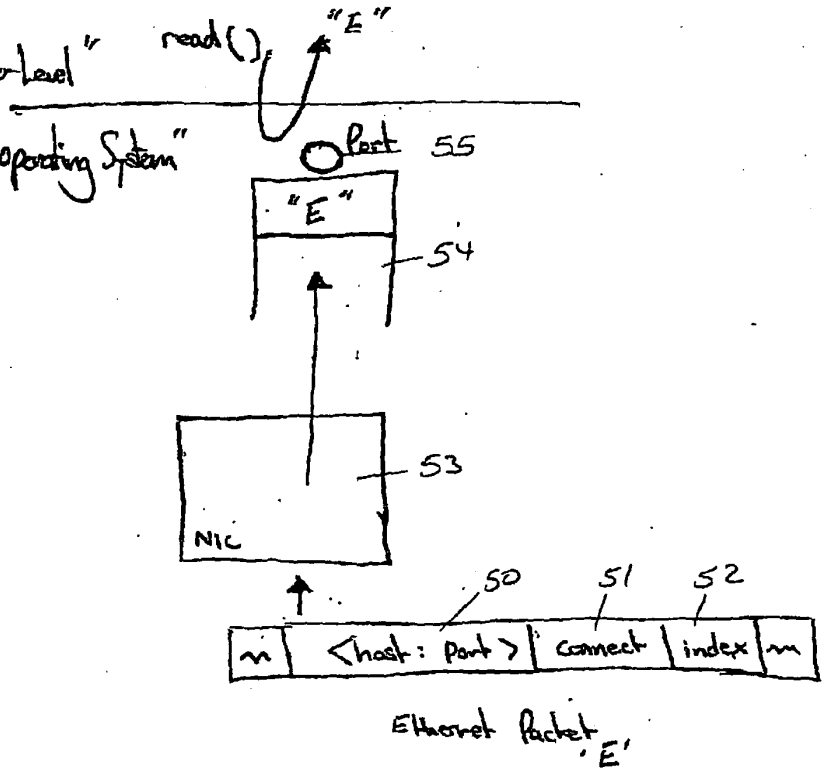
"User Level"
read()
"E"
"operating System"
Port 55
"E"
54
53
NIC
50
51
52
n
<host: port>
connect
index
m
Ethernet Packet 'E'

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Fig. 8

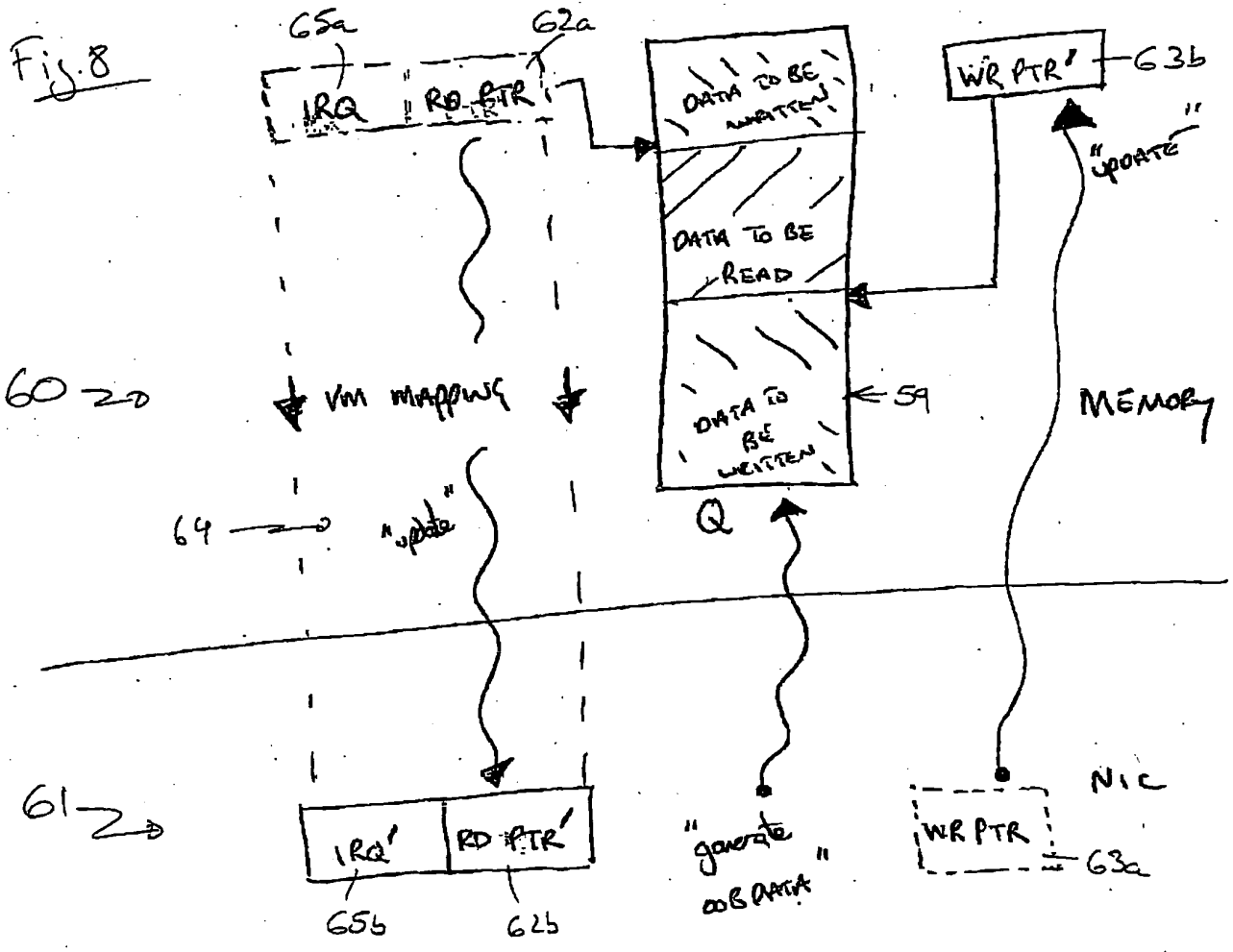
65a
62a
IRQ
RD PTR
DATA TO BE WRITTEN
DATA TO BE READ
DATA TO BE WRITTEN
WR PTR'
63b
"update"
60
VM MAPPING
59
MEMORY
64
"update"
Q
61
IRQ'
RD PTR'
"generate OOB DATA"
NIC
WR PTR
63a
65b
62b

Fig 9

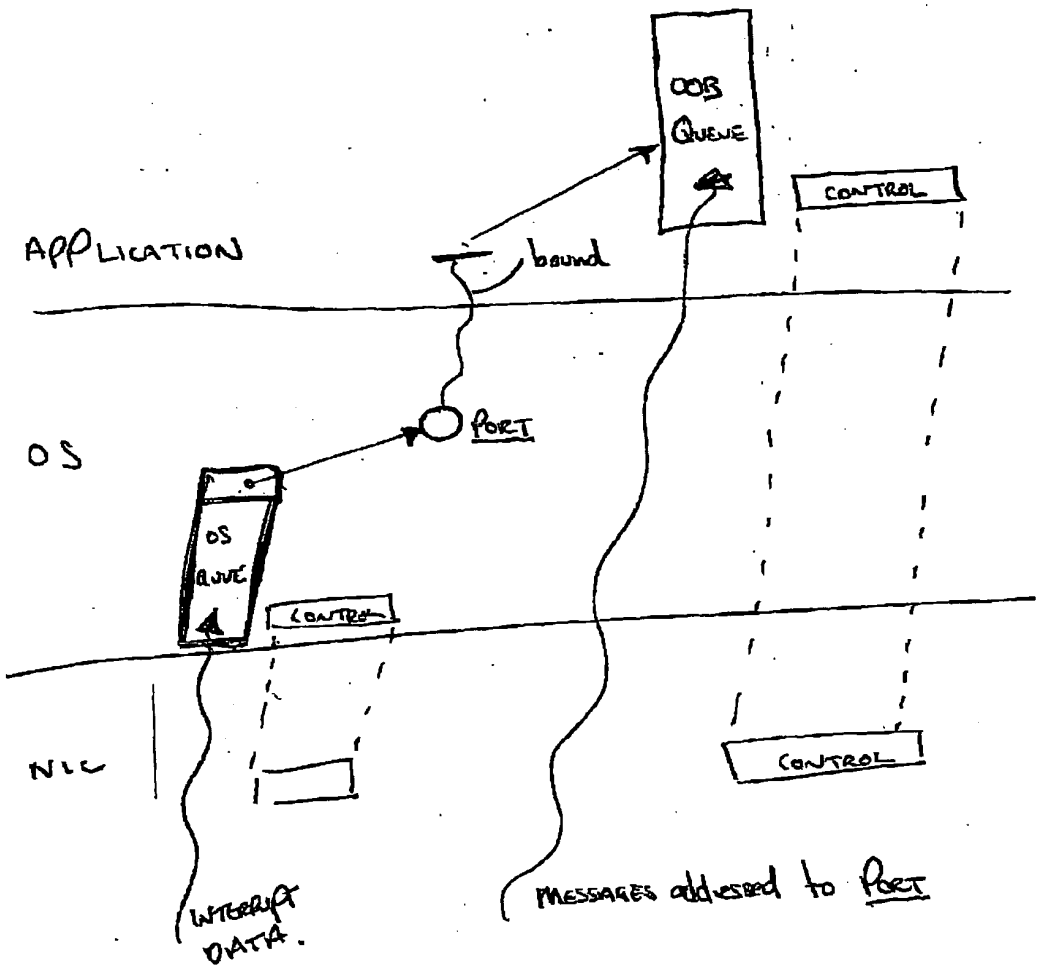
OOB
QUEUE
CONTROL
APPLICATION
bound
PORT
OS
OS
QUE
CONTROL
NIC
CONTROL
INTERRUPT
DATA.
MESSAGES addressed to PORT

Fig. 10

[NB order here not relevant]

			TYPE CI EVENT	PORT		SEQ number
BASE of PCI ADDRESS	48 BYTE DEST ETHERNET ADDRESS	16 bit DEST CLUSTER ADDRESS	TYPE CI	nonce	aperture index	SEQ number
"	"	4 byte DEST IP ADDRESS	TYPE IP	PORT		"

PCI → Ethernet Packet

OUTGOING APERTURES

Fig. 11

incoming apertures

aperture index	nonce	SEQ number	TYPE CI	Source cluster ADDRESS	Source Ethernet address	SIZE	Base of PCI address for aperture
PORT		SEQ number	TYPE CI Event	Source IP address	Source Ethernet address		Pointer to descriptor for Event queue
"		"	TYPE IP	"	"		Pointer to descriptor variable data queue

Ethernet Packet → PCI

Fig. 12

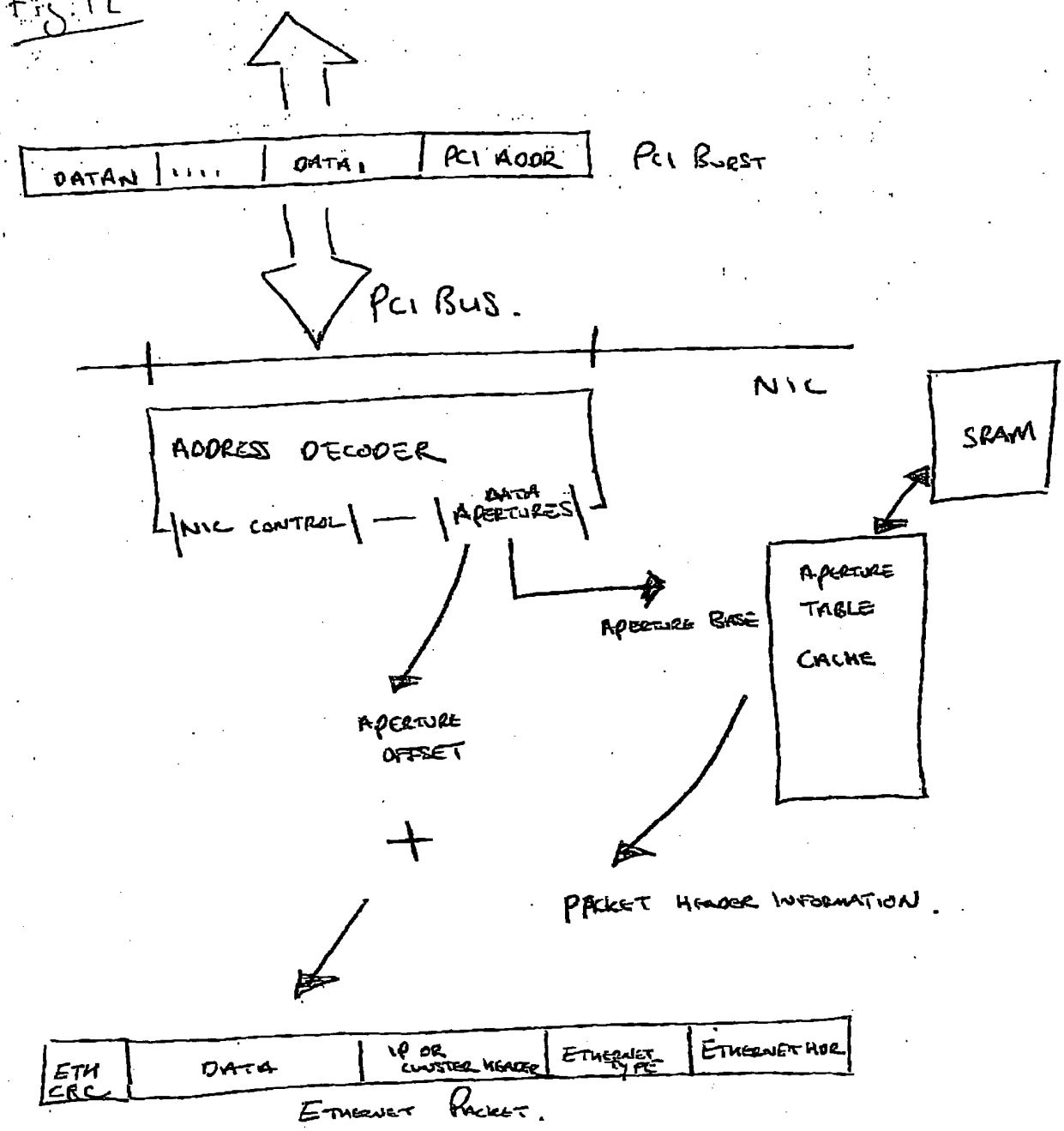
DATAN
....
DATA1
PCI HDDR
PCI BURST
PCI BUS.
NIC
ADDRESS DECODER
NIC CONTROL
DATA APERTURES
SRAM
APERTURE TABLE CACHE
APERTURE BASE
APERTURE OFFSET
+
PACKET HEADER INFORMATION.
ETH CRC
DATA
IP OR CLUSTER HEADER
ETHERNET TYPE
ETHERNET HDR
ETHERNET PACKET.

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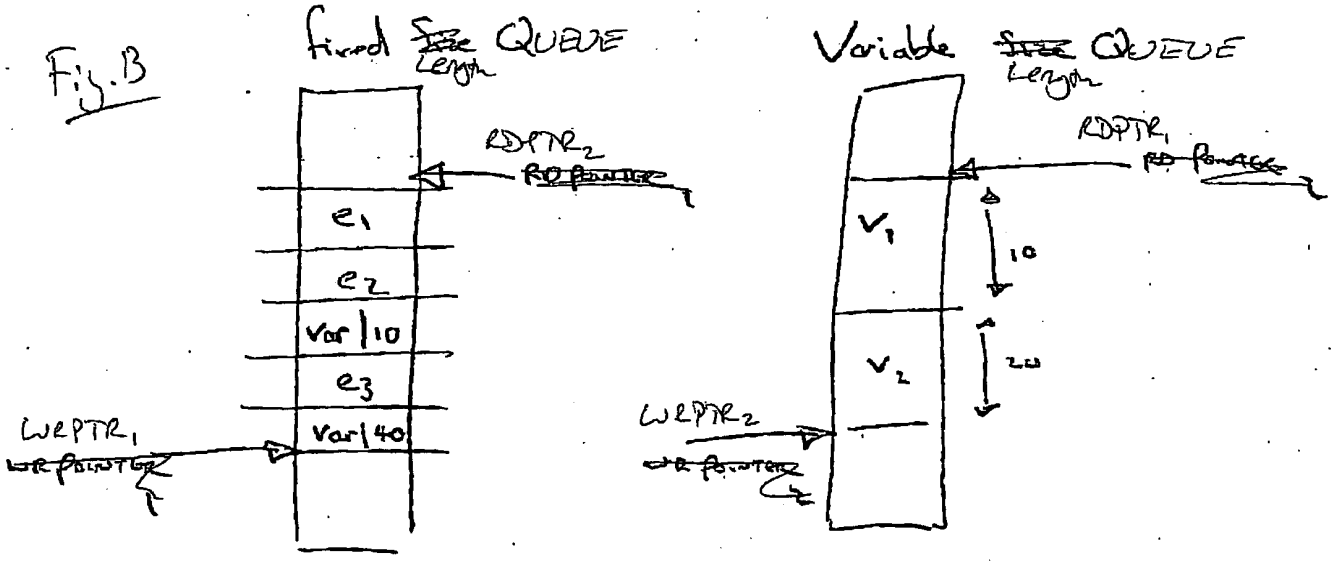
Fig. 3


fixed ~~Size~~ Length QUEUE
RDPTR2
e1
e2
Var | 10
e3
Var | 40
WRPTR1
Variable ~~Size~~ Length QUEUE
RDPTR1
V1
10
V2
20
WRPTR2